Q·Kernel
The new generation RTOS

White Paper Architecture

A new generation of RTOS is emerging that implements the segmented interrupt architecture. This architecture does not suffer from the limitations and problems of the more traditional RTOS.

The Traditional RTOS

Some of the biggest problems of the traditional RTOS is interrupt jitter, interrupt latency and the lack of an operating environment between ISR and threads. The traditional RTOS disables interrupts during critical sections. Every RTOS contains critical sections to access global data and to protect data from being modified by interrupt handlers. The largest critical sections are context switches which will disable interrupt handling for 60 to 120 cycles. While hardware vendors spend a lot of effort to minimize hardware interrupt latency (just 4 cycles for the dsPIC and PIC24) an RTOS adds sometimes more than 100 cycles to the interrupt latency.

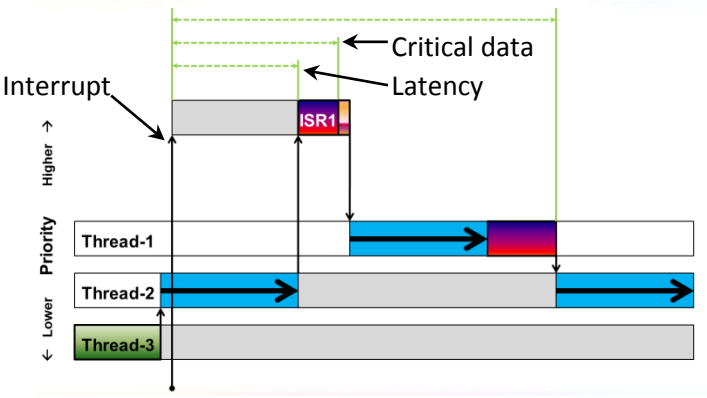
The Dual-Mode RTOS

Dual-Mode RTOS and other systems with segmented interrupt architecture don't disable interrupts, but will postpone communication with the RTOS when a critical section is detected. This approach solves the interrupt jitter and guarantees zero interrupt latency. A Dual-Mode RTOS uses a zone between ISRs and threads to handle high dataflow operations.

Case Study

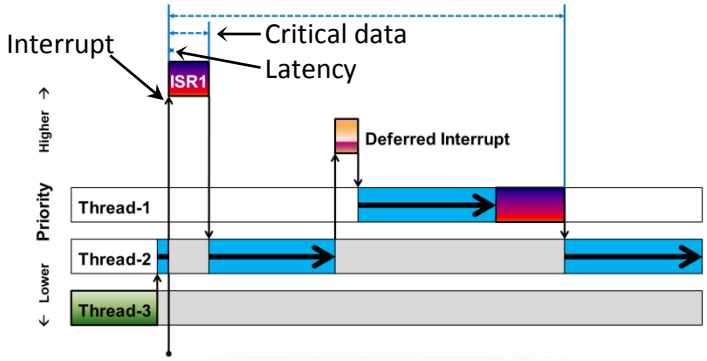
The case study describes interrupt handling during a critical section. The example below specifies a situation where there are three threads and one ISR. Thread-3 is active but is preempted by Thread-2 which has a higher priority. Thread-1 is waiting for data. The ISR consists of two parts – the first part of the ISR reads data from hardware registers and the second part of the ISR communicates this data to Thread-1. Context switches are represented in blue with a black arrow.

The Unified Architecture



Nothing happens when the interrupt occurs because interrupts are disabled during context switches. After the context switch, the ISR becomes active. It then executes another context switch to activate Thread-1.

The Segmented Architecture



When the interrupt occurs the ISR is activated and will read the hardware registers. The ISR can't communicate with the RTOS so it will defer that operation. This architecture outperforms the unified architecture in latency and reads critical data faster. The RTOS will queue the data for the deferred operation so it has no negative impact on performance.

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